Why  the insecurities?

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IoT Single System Image

- Unlike modern Oses, low end IoT devices have:
  - Limited flash
  - Severely Limited memory (64k!)
  - No MMU
  - Nothing we would consider an OS, really
- Programs are overlays, rather than tasks
- Billions of devices like these projected...
- What could go wrong??

A piece of IoT Code (from RiotOS)

```
void __attribute__((weak)) free(void *ptr)
{
    /* who cares about pointers? */
    (void) ptr;
    DEBUG("free(): block at %p lost.\n", ptr);
}
```

Be afraid, be very afraid.

My OSI 11 Layer Model

- 0: Historical
- 1: Physical
- 2: Data Link
- 3: Network
- 4 Transport
- 5: Session
- 6: Presentation
- 7: Application
- 8: Individual
- 9: Organizational
- 10: Government

But our big problems *Cross* Layers

- 0: Historical
- 1: Physical
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50 years of computer History

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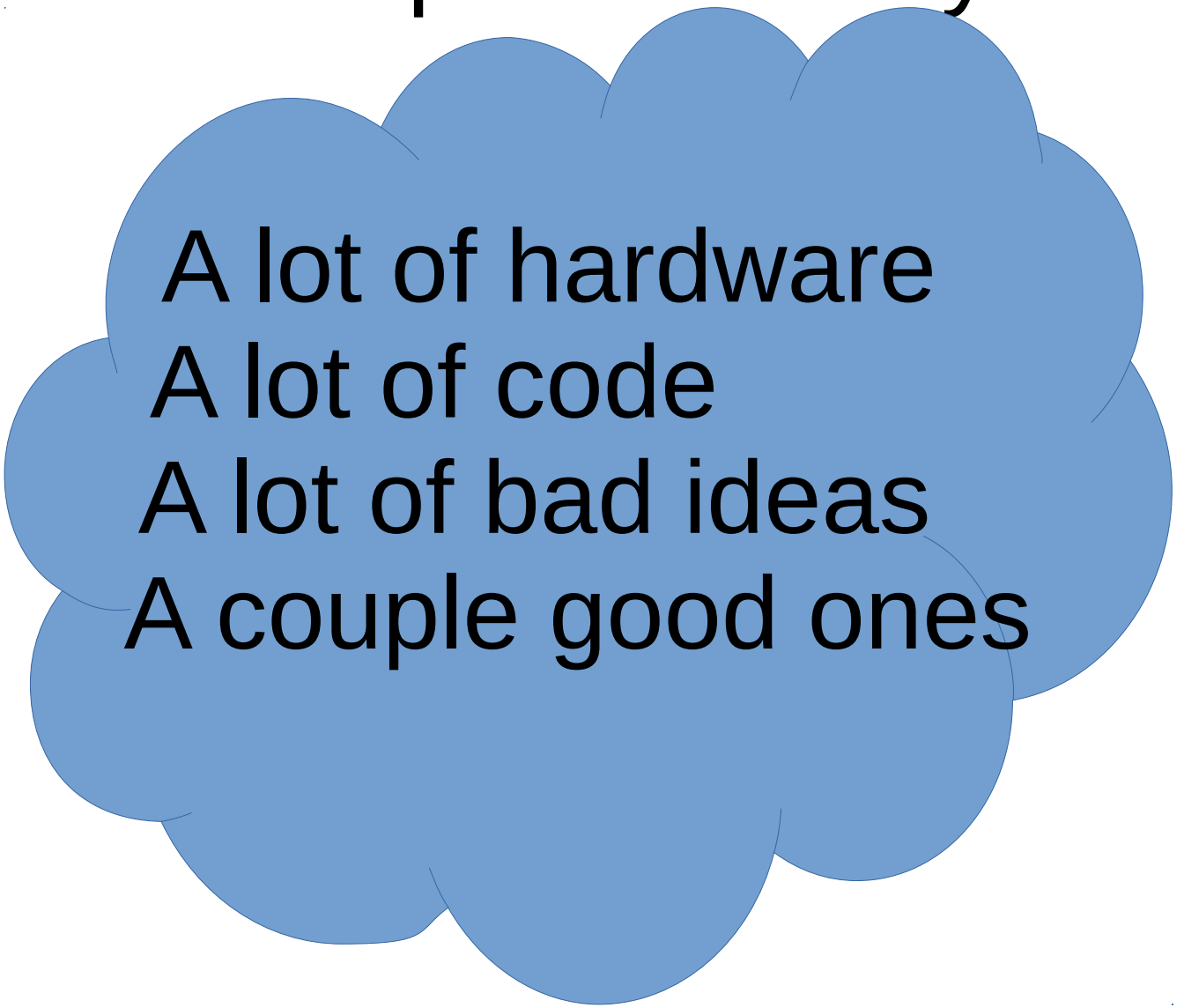
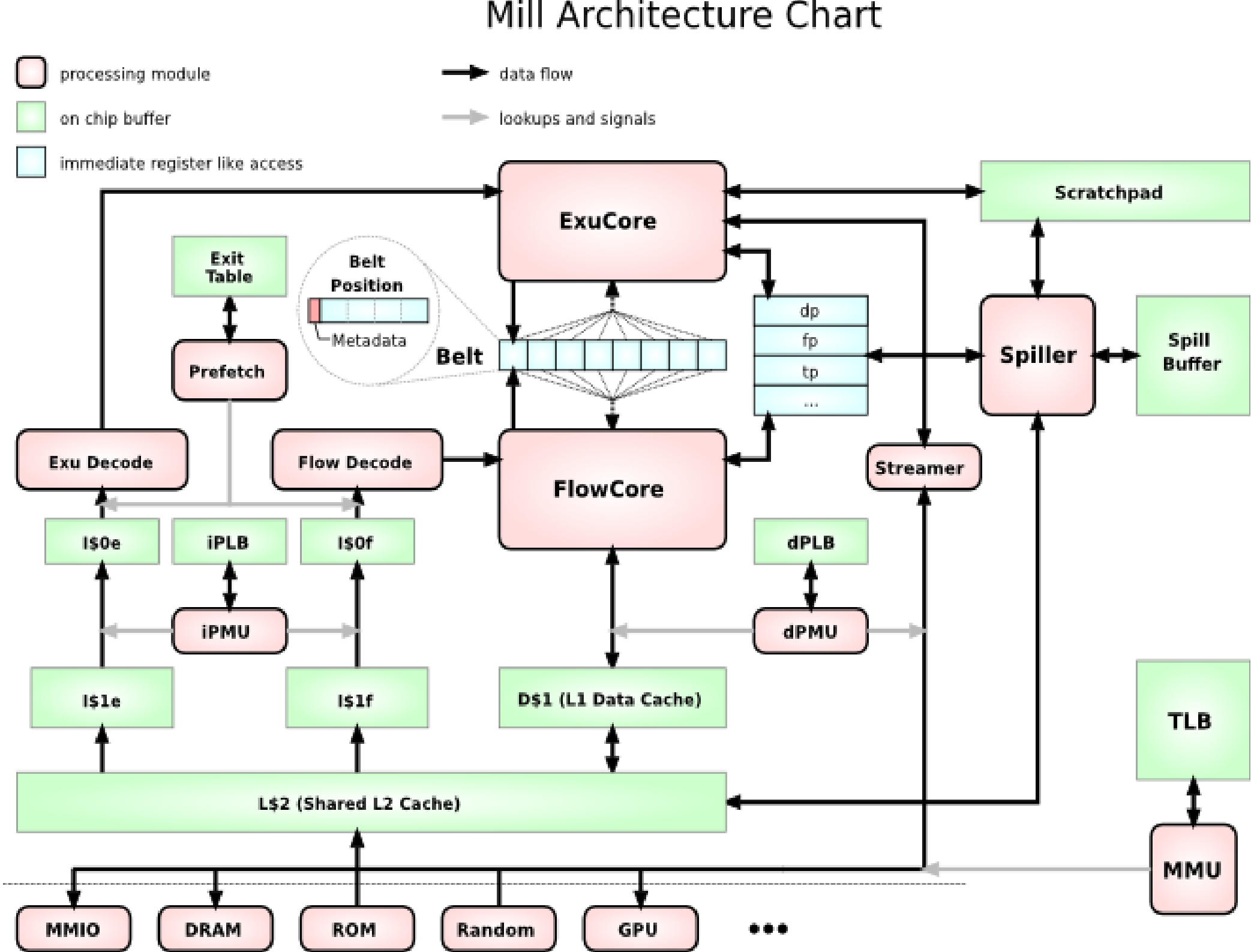


We **could** make better hardware

- But...
  - Hardware design languages and utilities are stuck in the 80s in terms of interoperability and reuse.
  - Chipmaking is widely viewed as a monopolists activity
  - Promising, more secure architectures vanquished by faster, cheaper ones
- Makers, everywhere, making stuff out of chips, but not making chips!
- FPGAs are cheap and getting cheaper
  - 28nm chip making processes are widely available
  - Even cpus – are now in the design scope of small teams –
    - see adapteva, neo, millcomputer, etc
- The system is rotten to its cores!
- We **can** make better cpus and circuits! OpenRisc, Risc-v already exist!
- Plenty of open VHDL/Verilog code available from opencores.org and elsewhere – but we **can** make better hardware design languages like Chisel!
- What would **you** do with 10 billion transistors?


Mill Architecture Chart
processing module
on chip buffer
immediate register like access
data flow
lookups and signals
ExuCore
Scratchpad
Exit Table
Belt Position
Metadata
Belt
Prefetch
dp
fp
tp
...
Spiller
Spill Buffer
Exu Decode
Flow Decode
FlowCore
Streamer
I$0e
iPLB
I$0f
dPLB
iPMU
dPMU
I$1e
I$1f
D$1 (L1 Data Cache)
TLB
L$2 (Shared L2 Cache)
MMU
MMIO
DRAM
ROM
Random
GPU
•••

The physical and Data link layers

- 0: Historical
- 1: Physical
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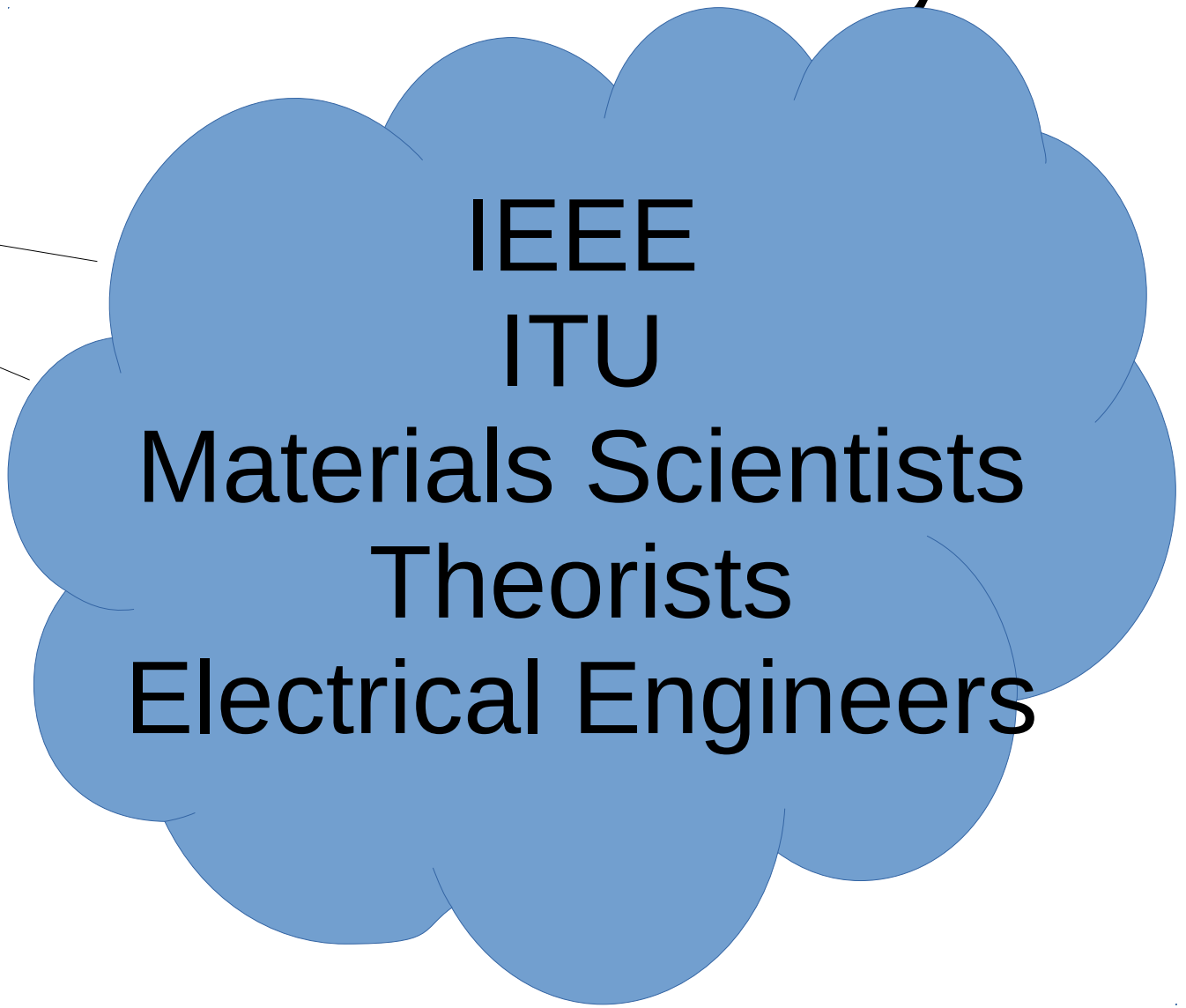

The Network and Transport Layers

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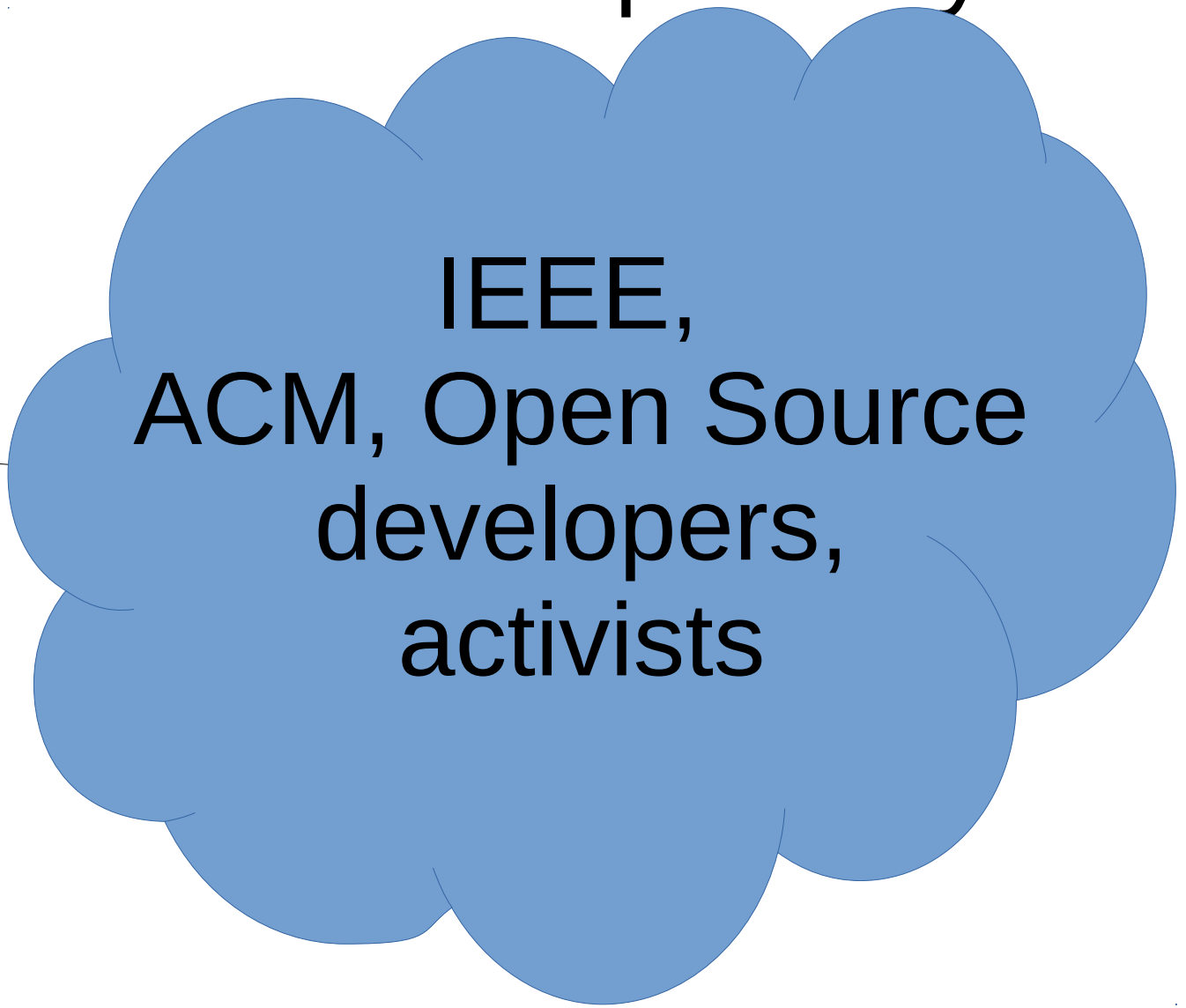

Session and Presentation “layers”

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Applications

- 0: Historical
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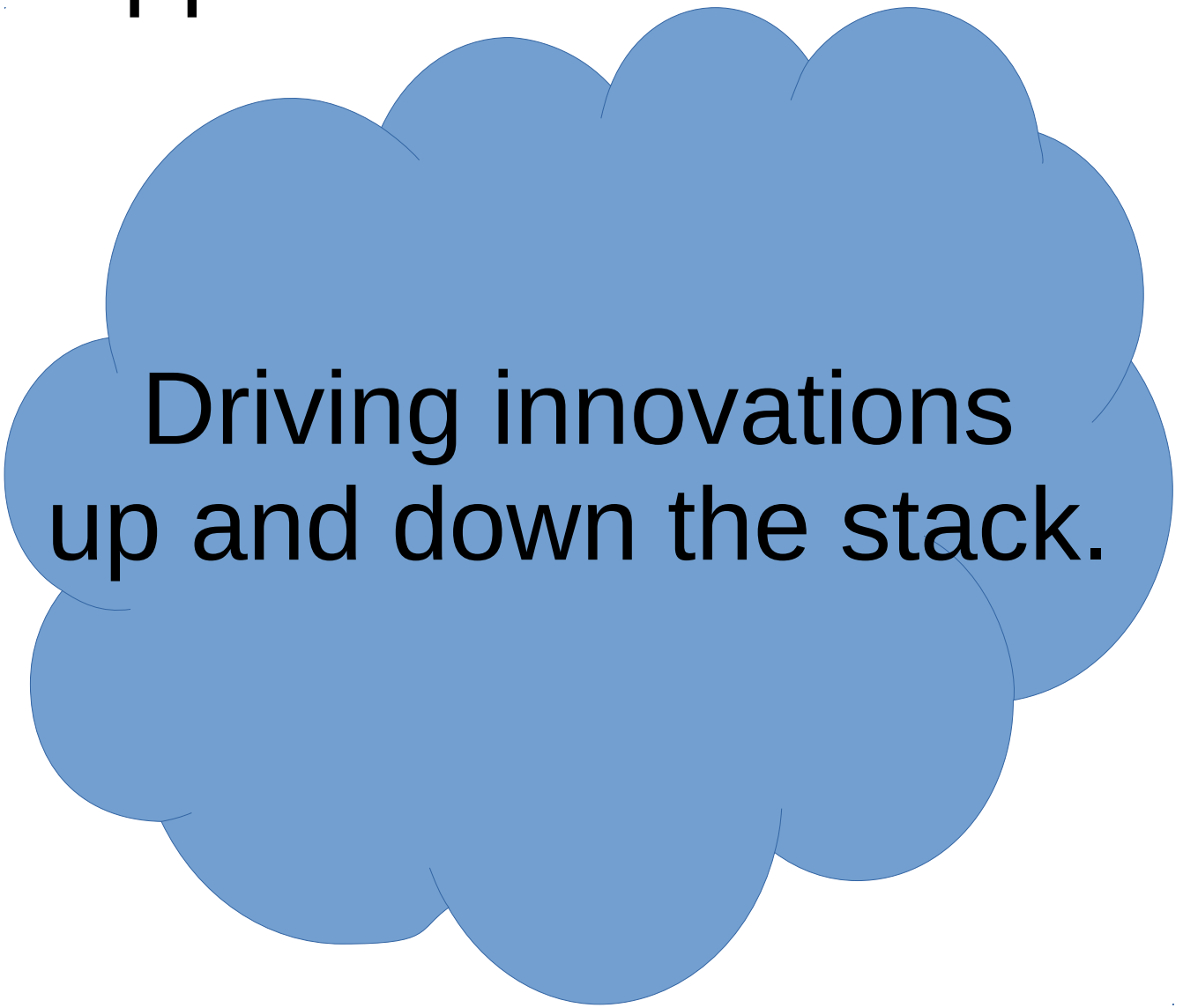

Individual, Organizational, Governance "Layers"

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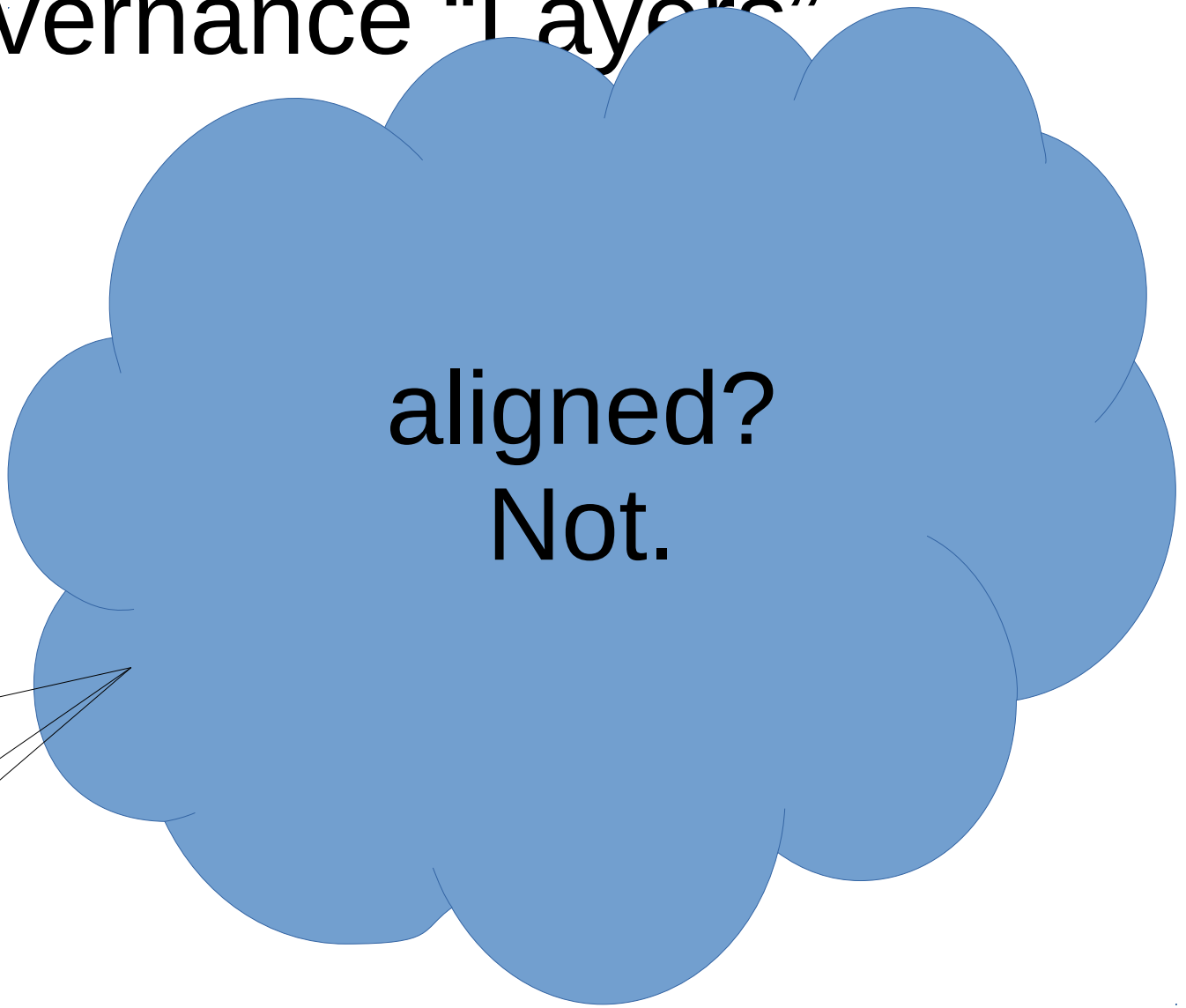
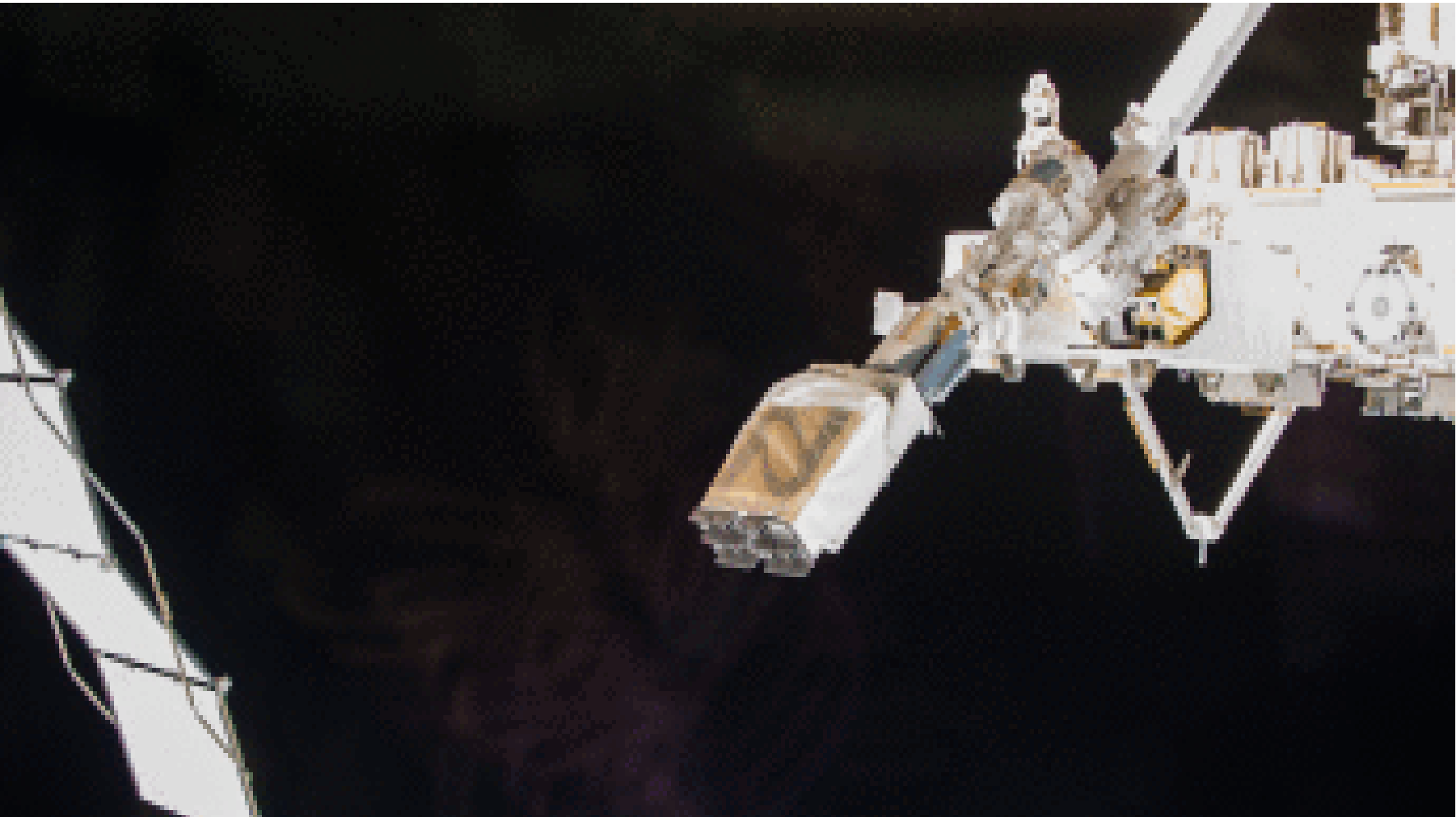


Action Items

- Hug an electrical engineer
- Take a politician out to dinner
- Attend a meeting out of your comfort zone
- And write the best code you can.

Arkyd 3 Cubesat Launch from the ISS (running linux)




Do good work!